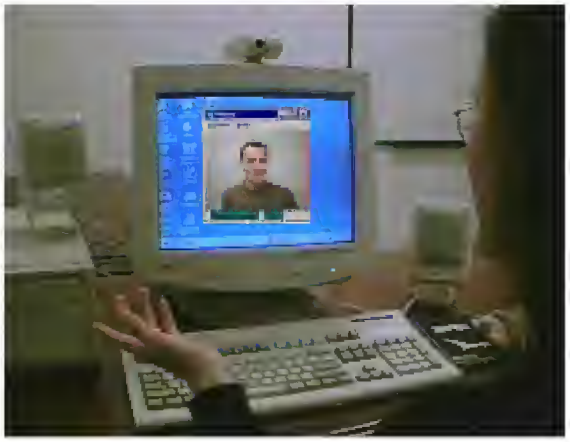
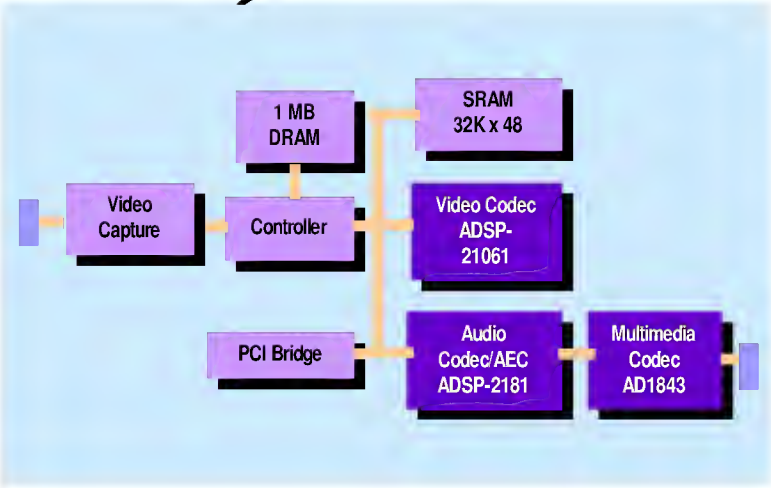
VideoCon H.324



The VideoCon H.324 reference design delivers videophone, videoconferencing and multimedia capabilities to any Pentium PC over analog telephone lines. The VideoCon H.324 performs all video compression and decompression on its included SHARC floating-point digital signal processor (DSP) and all audio compression and decompression on its included fixed-point DSP. The reference design only uses the Pentium processor for system control functions.

Highlights

- **Compliance with H.324 for POTS Videoconferencing**
- **Programmable support for MPEG, AC3 and High-End Audio for Multimedia applications**
- **Supports H.223 Data Framing, H.245 End-to-End Signaling and Indication/Control**
- **Supports G.723.1 at 6.3/5.3 kbps**
- **Includes 60-400 ms of Acoustic Echo Cancellation**
- **Supports Windows™95 API to enable User Customization of the Videoconferencing Application GUI**

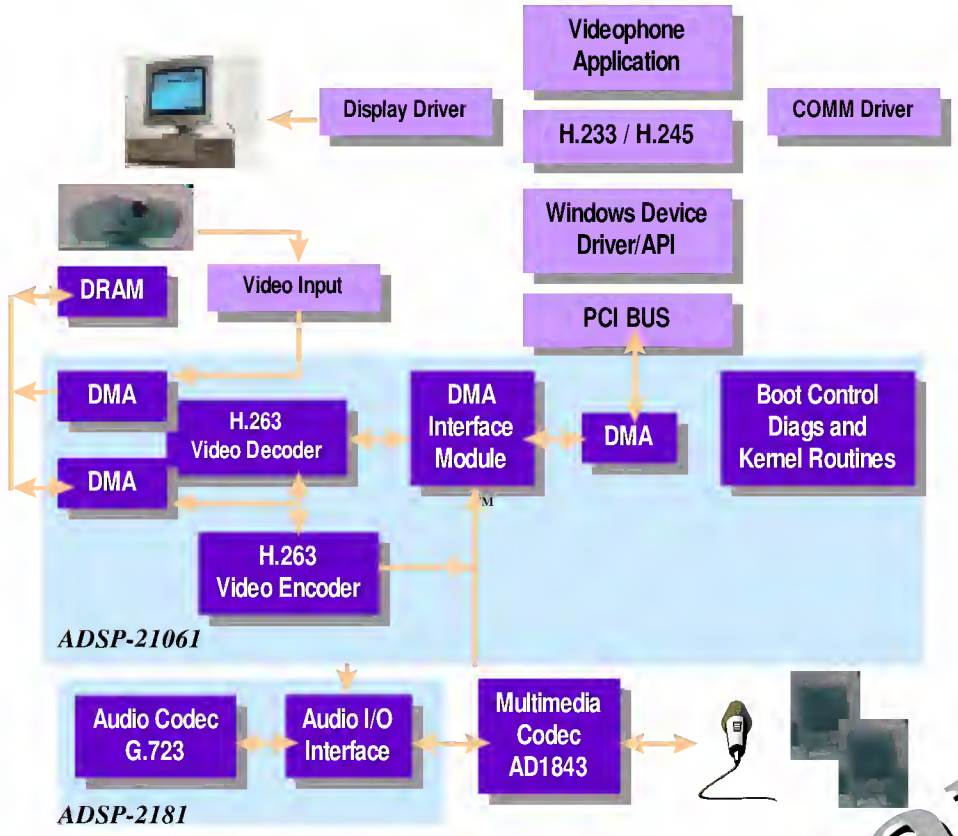


The VideoCon H.324 reference design implements the G.723.1 audio compression/ decompression algorithms on its on-board ADSP-2181 fixed-point DSP, the H.263 video compression/decompression algorithms on its on-board ADSP-21061 SHARC floating-point DSP, the V.34 modem algorithms on any external V.34 modem, and the H.223/245 system control algorithms on the host Pentium processor.

The reference design includes a board, software modules and development tools. The board is plugged into the PCI bus of the Pentium PC. The VideoCon H.324 – not the processor in the PC – performs the audio and video compression and decompression, audio acoustic echo cancellation, standards-compliant processing of audio, video, and telephony algorithms and programmable multimedia support for MPEG, Dolby AC-3 and high-end audio. The Pentium processor is used only for system control functions. The design supports the Windows™95 API to enable user customization of the videoconferencing application Graphical User Interface (GUI). The hardware components consist of Analog Devices' DSPs and media codecs for real-time application implementation.

The VideoCon H.324 design complies with the H.324 standard for POTS videoconferencing over analog telephone lines. The VideoCon H.324 architecture includes a high degree of hardware and software integration to reduce system cost as well as a reprogrammable media and communications architecture which can be upgraded to newer design implementations in the future.

The reference design includes a flexible set of software modules consisting of standards-compliant audio, video, telephony and system control algorithms. The VideoCon H.324 design provides advantages that proprietary, ASIC-based systems cannot match



PRODUCT DESCRIPTION

Analog Devices' VideoCon H.324 reference design is a hardware/software upgradable board for videoconferencing and multimedia applications. It is based on the ADSP-21061 to implement the video codec/system control and ADSP-2181 to implement audio codec/acoustic echo cancellation.

The incoming composite or S-VHS camera signal is converted to 4:2:2 YUV format by the frame grabber. When the ADSP-21061 is ready to encode the next frame, it sets up DMA channel 7 to transfer data, either in QCIF (176x144) or CIF (352x288 pixels) format from the frame grabber into the DRAM. The ADSP-21061 receives an interrupt at the end of the frame transfer.

Frame data is transferred on a macroblock by macroblock basis using DMA channel 9 from DRAM to internal SRAM of the ADSP-21061 for motion estimation and encoding.

The encoded bitstream is then multiplexed with G.723.1 audio bitsteam by the system controller. H.223 data framing, H.245 end-to-end signaling and control are all performed by the system controller. Video, audio and system controller data are then sent through the modem

The H.324 bitstream is transferred to the system controller where video and audio data are demultiplexed and transferred to the respective decoders. The video bitstream is decoded by the ADSP-21061 and passed in 4:2:0 format to the host using DMA channel 6. YUV to RGB format conversion is performed either by the host or by the graphics controller. Data to and from the reconstructed frame buffer is transferred in and out of the internal memory using DMA channel 9.

The ADSP-2181 implements the audio codec and acoustic echo cancellation. Speech signals are digitized by the AD1843 and transferred to the ADSP-2181 echo cancellation module with a capability to cancel 60 to 400 ms of acoustic echo. The data is then encoded, lip synchronized with video and transferred to the system controller for multiplexing with video data. Demultiplexed audio is transferred to the ADSP-2181 to be decoded. Decoded data is lip synchronized with video and played back through the ADSP-1843. Communication between the ADSP-21061 and AD2181 is through the IDMA port of the ADSP-2181.

VIDEOCON H.324 SPECIFICATIONS

FUNCTIONAL SPECIFICATIONS

System Control
H.223 for Framing, Multiplex, Error Control
H.245 for End to End Signaling, Capability Exchange

Video Codec
H.263
Source Format: SQCIF, QCIF, CIF
Motion Estimation
Half-Pixel Interpolation
PB Frames
Optional Error Correction

Audio Codec
Narrow Band (8 KHz Sampling): G.723.1 @ 5.3/6.3 Kbps

Dynamic Mode Switching
Symmetrical and Asymmetrical Audio Modes

Acoustic Echo Cancellation
60-400 ms depending on Audio mode

Network Interface
28.8 Kbps (V.34)

Application Areas
Videoconferencing, Security/Surveillance, Distance learning, Video mail, Set-Top Boxes, Telemedicine

HARDWARE SPECIFICATIONS

Processing Engines
ADSP-21061 @ 40 MHz for Video Codec
ADSP-2181 @ 33 MHz for Audio Codec & Acoustic Echo Cancellation
Pentium @60 MHz (minimum) for System Control

External Memory
256 k x 16 x 2-60 ns DRAM
- 4 Cycles Page Miss
- 2 Cycles Page Hit

Refresh: CAS before RAS
- 4 Cycles @12.5 µ s

ADSP-2181 Interface
16-Bit IDMA Port Access
Core Access or DMA Access
2 Cycle Index Address Write
2 Cycle Data Read/Write
Synchronous Serial Interface
- SPORT 1 (ADSP-2181) to SPORT 1 (ADSP-21061)

Handshake Interrupts
ADSP-21061 to ADSP-2181 INTERRUPT
ADSP-2181 to ADSP-21061 INTERRUPT

Audio I/O
Controller: AD1843 SoundComm
Inputs: Microphone - 1 Channel for Dynamic or Condenser Microphone
Outputs:
- Speaker - 1 W @ 8 Ohms
- Modem Support V.32 bis,

Sampling Rates: 4 kHz to 54 kHz
Gain: Programmable
Attenuation: Programmable
Mute: Programmable
Filters: On-Chip Digital Interpolation Decimation and O/P Low-Pass Filter 3 On-Chip PLL's
Host Interface: TDM Serial Master Mode to SPORT of ADSP-2181

Video Digitization
Digitizer: Bt 819
Input: PAL/NTSC Composite Video 1
- RCA Phono Input

Scaling - Horizontal: 6 TAP Interpolation
Scaling - Vertical: 2 TAP Interpolation
Picture Control: Programmable
- Brightness, Contrast, Hue, Saturation, Luma Decimation Filter

Control Interface: I2C
Interrupt Generation: Frame Store

ANALOG DEVICES

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